A 10 Gb/s CDR in SiGe BiCMOS commercial technology with multistandard capability

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Abstract — **A 10Gb/s CDR in SiGe BiCMOS technology featuring multistandard compliance with SDH/SONET and 10GbE specs and generated jitter below 65mUIpp is presented. The CDR features a 20mV-sensitivity limiting amplifier, a 2-DFF-based decision circuit to maximize CPM and a dual loop PLL architecture with external reference clock and a novel PD topology. Power consumption is below 780mW from 2.5 and 3.3 V supplies.**

I. Introduction

In recent years it has been observed a widespread diffusion of high bit-rate optical communication systems for both long distance telecom transport networks and short-haul datacom systems. Optical transmission technologies have completely taken over the backbone and transport network segments thanks to their unparalleled performance, and the advent of multimedia applications has spurred the demand of higher-capacity fiber-based LANs. 10Gb/s is nowadays the highest bit-rate used in commercially available serial data links, and it is covered by different standards, both for long-distance telecom systems (SDH/SONET [1]-[2]) and for datacom LANs and MANs (IEEE 10 Gigabit Ethernet [3]).

Network components demand for low cost, high productivity, small size and low power consumption; for short-haul systems such as LANs and the access network in particular, an important consideration is cost competitiveness. In this scenario, the availability of multi-standard-compatible building blocks can greatly contribute to cost and time-to-market reduction.

In this paper we present a SiGe 3.3V 10Gb/s Clock and Data Recovery (CDR) IC that can be used with all the main standards for 10Gb/s optical communications, i.e. SDH STM-64 / SONET OC-192 (9.953Gb/s), SDH / SONET with forward error correction (10.664Gb/s, 10.704Gb/s) and IEEE 10 Gigabit Ethernet (10.3125Gb/s). Section II presents the system-level design of the clock recovery circuit, Section III describes the circuit design of the main building blocks, Section IV gives some technological details and Section V shows the results of measurements.

II. Clock Recovery System Design

Clock recovery system design is dictated by jitter performance, that can be specified considering three issues: jitter generation, jitter transfer and jitter tolerance. SDH/SONET jitter specifications [2] have been taken into account, since they impose more stringent requirements. To satisfy the high-frequency jitter tolerance behavior, a CDR bandwidth of at least 4MHz is required, but as already shown in [4], this is in conflict with the jitter transfer bandwidth of 120kHz which is requested in optical regenerators, and that can be obtained by using an additional low-bandwidth PLL in the transceiver module. For this reason jitter tolerance, jitter generation (less than 0.1UIpp in 50kHz – 80MHz) and jitter transfer peaking (less than 0.1dB) have been the CDR design goals. A very large PLL bandwidth would be beneficial to minimize jitter generation, but we have preferred to limit the bandwidth below 8MHz, to conform to a *de facto* standard that is an extrapolation from ITU specifications for lower bit-rates Type A regenerators. A bandwidth adjustment pin has been added to allow satisfying jitter specifications over all process, supply voltage and temperature (PVT) conditions.

The main sources of jitter transfer peaking can be found in the PLL phase margin and in the closed-loop doublet. To have a closed-loop transfer function with less than 0.1dB peaking, a phase margin better than 60° has been obtained by setting the high frequency parasitic poles in the loop at sufficient higher frequency with respect to the PLL bandwidth. The additional source of peaking is the pole-zero doublet in the PLL transfer function, whose contribution is minimized when the frequency of the zero, that has been set to 10kHz, is much lower than the PLL bandwidth.

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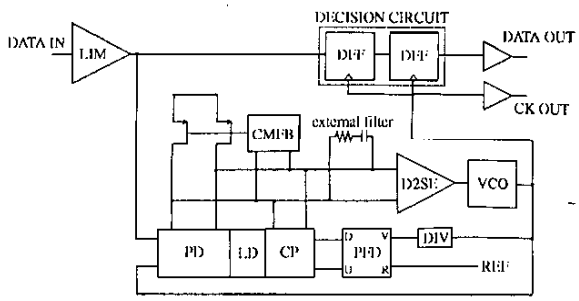

Fig. 1. CDR IC block diagram (LD: lock detector; other acronyms are defined in the text).

To overcome the small acquisition range due to the limited loop bandwidth, the clock recovery has been implemented by a dual loop PLL architecture: a first loop locks the VCO to an external low frequency reference clock; after that, this loop is switched off and the second loop is activated to lock the VCO to the phase of the incoming data. A 16/64 programmable feedback divider allows the use of two different families of reference clock sources: 155-167MHz and 621-656MHz.

III. CDR Circuit Design

The block scheme of the IC is shown in Fig. 1: it consists of a 66dB-gain limiting amplifier (LIM) which receives the incoming NRZ data stream, a dual-loop PLL-based clock recovery unit and a decision circuit. The recovered data and clock are made available by two 50Ω CML output buffers.

The acquisition loop consists of a phase-frequency detector (PFD), a charge pump (CP) and a 16/64 programmable divider, and it shares the VCO, the differential loop filter and the differential to single-ended converter (D2SE) with the phase tracking loop. The PLL is fully integrated except for the differential loop filter, which consists of an external resistor and capacitor series.

The acquisition loop reuses blocks already designed for a Clock Multiplier Unit (CMU) for the transmission side of the link. A CML semi-synchronous frequency divider [5] has been chosen as a trade-off between phase noise performance and high speed requirements. A standard three-state PFD with a differential charge-pump have been implemented in CML logic to minimize jitter due to mismatches.

A. Voltage-controlled oscillator

To achieve low phase noise, the VCO has been implemented with a LC-tank topology with capacitive tapping (Fig. 2) [6]. The integrated inductors have been designed as spiral inductors implemented in the top metal

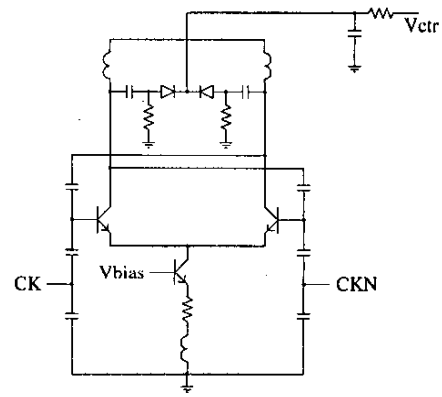

Fig. 2. Voltage-controlled oscillator.

layer (2.5μm thickness), with patterned ground shields to reduce substrate losses. VCO tuning is performed by means of two P+/Nwell varactor diodes, driven by the D2SE output.

To overcome the issue of the very limited tuning range (about 12%) provided by LC VCOs, two VCOs centered at 9.8 and 10.45GHz have been integrated on the chip, so allowing the CDR to operate with the different standards for 10Gb/s transmission over all PVT conditions.

B. D2SE amplifier

The D2SE amplifier has been designed with about 100MHz bandwidth, not to degrade the loop phase margin; moreover, low noise, high CMRR and PSRR and rail-to-rail output have been targeted. It consists of a high common-mode rejection low-leakage unity-gain CMOS differential stage, followed by a 9.5dB-gain difference amplifier whose gain has been fixed as a trade-off between low noise requirements and the need to limit the voltage swing on the loop filter (see Fig. 3).

C. Phase detector

Self-aligned phase detector (PD) architectures (e.g Hogge PD [7]) at high frequencies suffer from the effect of finite transit times of D-type flip-flop circuits, so that a

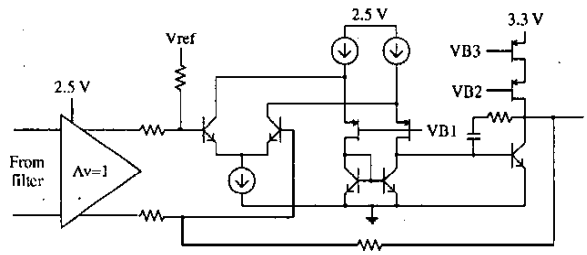

Fig. 3. D2SE amplifier.

non-zero static phase error is present and data-clock alignment at the decision circuit relies on delay matching between different paths [8].

To minimize jitter contribution we have preferred to use a sinusoidal DRML-like phase detector structure [9]; clock-data alignment at the decision circuit relies on delay matching between the different signal paths and on static phase offset compensation. A low-jitter sampling-type phase detector based on a novel topology has been designed, featuring a current-mode output to simplify sharing the same loop filter with the current-mode charge pump. This allows a tri-state behavior with zero output current when no data transition is present.

D. Decision circuit

A 30ps budget has been assigned to cover the overall misalignment between clock and data at the decision circuit; the main sources, whose contribution adds to the generated jitter, can be found in the PD static phase error, and in the finite clock phase margin (CPM) of the decision circuit. The PD static phase error has been compensated by adding delay elements on the clock path. On the other hand, the CPM of the decision circuit has been optimized by using a cascade of two master-slave D-type CML flip-flops (DFF), as shown in Fig. 1: the first flip-flop takes decision on the input data stream, but its output swing could result in low signal for very strong misalignments between clock and data; for this reason a second flip-flop has been added to act as a clocked comparator to reopen the eye and to retime the data stream. This allows a net enhancement of the clock phase margin of the overall decision circuit, leaving more margin to the other misalignment sources and maximizing the jitter tolerance.

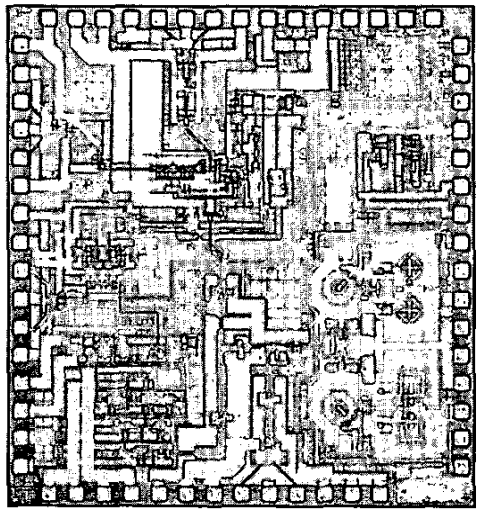

Fig. 4. Die micrograph.

IV. Technological Details

The CDR has been integrated in STMicroelectronics BiCMOS7 technology [10], that is a SiGe HBT/CMOS technology suitable for RF system-on-chip applications.

The technology features high-frequency SiGe bipolar devices (f_T>65GHz, β=100, BV_{CEO}=2.6V, V_A>50V) together with a 0.25μm CMOS and a large set of passive components (resistors, MIM and MOS capacitors, varactors and spiral inductors). Five metal layers are provided for interconnections, with the top level optimized for the implementation of high-Q inductors.

Two power supplies have been used: 3.3V for VCO and CML design (PFD, divider, data path, decision circuit), and 2.5V for low-frequency digital blocks (lock detector) and CMOS analog design (PD, charge pump, D2SE); separate power supplies have been used to minimize high frequency coupling between critical blocks.

Fig. 4 shows a microphotograph of the chip, whose die size is 2.5x2.7mm^2.

V. Measurements Results

The IC has been mounted bare die on a PCB for testing, together with the external loop filter, supply decoupling networks and dip switches for VCO and division ratio selection. The overall current consumption is about 240mA from 3.3V and 2.5V supplies (780mW total power dissipation).

The IC input sensitivity is less than 20mVpp at BER=10^{-12} for a PRBS 2^{31}-1 single-ended input data stream. Fig. 5 shows the output data and clock waveforms

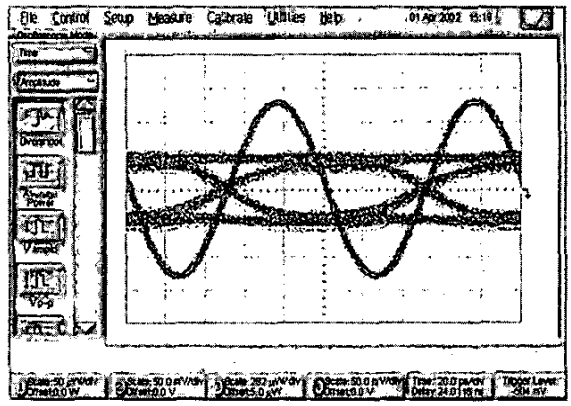

Fig. 5. Output data and clock waveforms at 9.95 Gb/s.

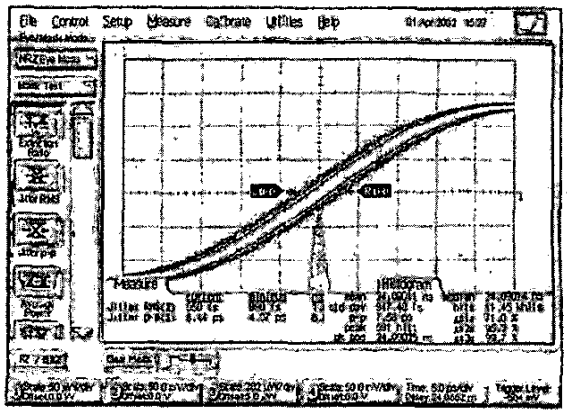

Fig. 6. Clock jitter histogram at 9.95 Gb/s.

for a 50mVpp input signal at 9.953Gb/s, and Fig. 6 shows the corresponding clock jitter histogram. Similar results have been obtained for 10.3 and 10.8Gb/s data streams.

Both VCOs have been tested, by setting to the appropriate value the dip switches on the board; the measured acquisition ranges have resulted in 9.43 - 10.25 GHz and 10.07 – 10.92GHz respectively, with a locking range always in excess of 200ppm.

Measurements have shown full compatibility with the jitter specifications for SONET OC-192: the generated jitter results about 65mUIpp when measured with the filter specified in [2]; the PLL transfer function (Fig. 7) presents no peaking, while being set between 4MHz and 8MHz. Fig. 8 shows the measured jitter tolerance behavior compared to the OC-192 mask for a PLL bandwidth of 4MHz.

VI. Conclusion

A fully monolithic 10Gb/s Clock and Data Recovery (CDR) IC featuring multistandard compliance with SDH/SONET and 10GbE specifications has been successfully implemented in a production level SiGe BiCMOS technology. A novel phase detector topology has been exploited to achieve good jitter performance and minimize pattern-dependent effects. Compliance with SONET OC-192 specifications has been successfully checked on a PCB-mounted version of the IC.

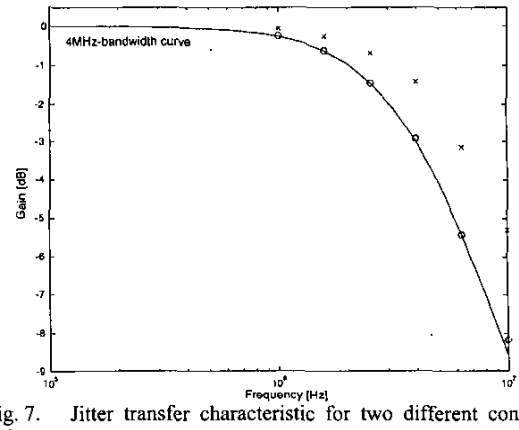

Fig. 7. Jitter transfer characteristic for two different control voltages.

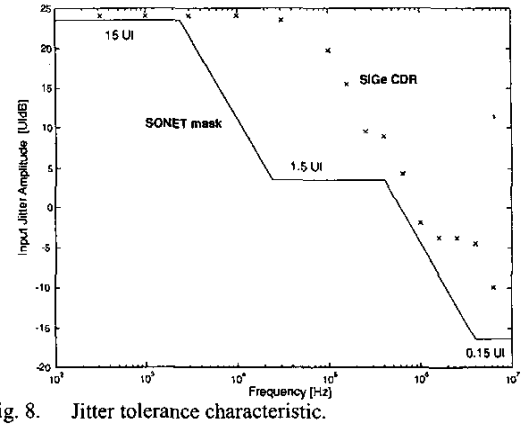

Fig. 8. Jitter tolerance characteristic.

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